ANNA UNIVERSITY, CHENNAI
NON- AUTONOMOUS COLLEGES AFFILIATED ANNA UNIVERSITY
M.E. VLSI DESIGN

REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM

1. **PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):**

- To critically analyse and understand the principles involved in the designing and testing of electronic circuits relevant to industry and society.
- To appreciate the concepts in the working of electronic circuits.
- To take up socially relevant and challenging projects and to provide Innovative solutions through research for the benefit of the society with latest hardware & software related to VLSI and also to develop the capacity to protect Intellectual Property.
- To Progress and Develop with Ethics and Communicate effectively.
- To become entrepreneurs to develop indigenous solutions.

2. **PROGRAM OUTCOMES (POs)**

1. An ability to independently carry out research/investigation and development work to solve practical problems

2. An ability to write and present a substantial technical report/document

3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

4. Understand the fundamentals involved in the Designing and Testing of electronic circuits in the VLSI domain.

5. Provide solutions through research to socially relevant issues for modern Electronic Design Automation (EDA) tools with knowledge, techniques, skills and for the benefit of the society

6. Interact effectively with the technical experts in industry and society

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M.E. VLSI DESIGN
REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM
I TO IV SEMESTERS CURRICULA AND 1st SEMESTER SYLLABI
SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4153	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2.	RM4151	Research Methodology and IPR	RMC	2	0	0	2	2
3.	VL4151	Analog IC Design	PCC	3	0	0	3	3
4.	VL4152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
5.	AP4152	Advanced Digital System Design	PCC	3	0	2	5	4
6.	AP4153	Semiconductor Devices and Modeling	PCC	3	0	0	3	3
7.		Audit Course – I*	AC	2	0	0	2	0
PRACTICALS								
8.	VL4111	FPGA Laboratory	PCC	0	0	4	4	2
9.	VL4112	Analog IC Design Laboratory	PCC	0	0	4	4	2
			TOTAL	**19**	**1**	**10**	**30**	**23**

*Audit course is optional

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4251	Design for Verification using UVM	PCC	3	0	0	3	3
2.	VL4291	Low Power VLSI Design	PCC	3	0	0	3	3
3.	VL4292	RFIC Design	PCC	3	0	0	3	3
4.	VL4252	VLSI Testing	PCC	3	0	0	3	3
5.		Professional Elective I	PEC	3	0	0	3	3
6.		Professional Elective II	PEC	3	0	0	3	3
7.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
8.	VL4211	Verification using UVM Laboratory	PCC	0	0	4	4	2
9.	VL4212	Term Paper Writing and Seminar	EEC	0	0	2	2	1
			TOTAL	**20**	**0**	**6**	**26**	**21**

*Audit course is optional

SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4351	VLSI Signal Processing	PCC	3	0	0	3	3
2.		Professional Elective III	PEC	3	0	0	3	3
3.		Professional Elective IV	PEC	3	0	2	5	4
4.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
5.	VL4311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**14**	**26**	**19**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	VL4411	Project Work II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 75

PROFESSIONAL ELECTIVES
SEMESTER II, ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4071	ASIC Design	PEC	3	0	0	3	3
2.	VE4152	Embedded System Design	PEC	3	0	0	3	3
3.	EL4071	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
4.	VL4001	Data Converters	PEC	3	0	0	3	3
5.	VL4002	Hardware Software Co-Design for FPGA	PEC	3	0	0	3	3
6.	IF4094	Pattern Recognition	PEC	3	0	0	3	3

SEMESTER II, ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4003	DSP Structures for VLSI	PEC	3	0	0	3	3
2.	VL4004	Power Management and Clock Distribution Circuits	PEC	3	0	0	3	3
3.	VL4005	Reconfigurable Architectures	PEC	3	0	0	3	3
4.	VL4006	Advanced Wireless Sensor Networks	PEC	3	0	0	3	3
5.	AP4095	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
6.	II4092	System On Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4073	MEMS and NEMS	PEC	3	0	0	3	3
2.	VL4091	Network on Chip	PEC	3	0	0	3	3
3.	CU4076	VLSI for Wireless Communication	PEC	3	0	0	3	3
4.	VL4074	Nanotechnology	PEC	3	0	0	3	3
5.	VL4007	Evolvable Hardware	PEC	3	0	0	3	3
6.	VL4092	Soft Computing and Optimization Techniques	PEC	3	0	0	3	3
7.	VL4072	CAD for VLSI Design	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4009	VLSI Architectures for Image Processing	PEC	3	0	2	5	4
2.	VL4010	System Verilog	PEC	3	0	2	5	4
3.	VL4011	Adaptive Signal Processing	PEC	3	0	2	5	4
4.	CP4252	Machine Learning	PEC	3	0	2	5	4
5.	DS4151	Digital Image and Video Processing	PEC	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	AX4091	English for Research Paper Writing	2	0	0	0
2.	AX4092	Disaster Management	2	0	0	0
3.	AX4093	Constitution of India	2	0	0	0
4.	AX4094	நற்றமிழ் இலக்கியம்	2	0	0	0

FOUNDATION COURSES (FC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VL4153	Graph Theory and Optimization Techniques	3	1	0	4	I

PROFESSIONAL CORE COURSES (PCC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VL4151	Analog IC Design	3	0	0	3	I
2.	VL4152	Digital CMOS VLSI Design	3	0	0	3	I
3.	AP4152	Advanced Digital System	3	0	2	4	I
4.	AP4153	Semiconductor Devices and Modeling	3	0	0	3	I
5.	VL4111	FPGA Laboratory	0	0	4	2	I
6.	VL4112	Analog IC Design Laboratory	0	0	4	2	I
7.	VL4251	Design for Verification using UVM	3	0	0	3	II
8.	VL4291	Low Power VLSI Design	3	0	0	3	II
9.	VL4292	RFIC Design	3	0	0	3	II
10.	VL4252	VLSI Testing	3	0	0	3	II
11.	VL4211	Verification using UVM Laboratory	0	0	4	2	II
12.	VL4351	VLSI Signal Processing	3	0	0	3	III

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	RM4151	Research Methodology and IPR	2	0	0	2	1

EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			Lecture	Tutorial	Practical		
1.	VL4212	Mini Project with seminar	0	0	2	1	II
2.	VL 4311	Project Work I	0	0	12	6	III
3.	VL 4411	Project Work II	0	0	24	12	IV

SUMMARY

Sl. No.	NAME OF THE PROGRAMME: M.E.VLSI DESIGN					
	SUBJECT AREA	CREDITS PER SEMESTER				CREDITS TOTAL
		I	II	III	IV	
1.	FC	04	00	00	00	04
2.	PCC	17	14	03	00	34
3.	PEC	00	06	07	00	13
4.	RMC	02	00	00	00	02
5.	OEC	00	00	03	00	03
6.	EEC	00	01	06	12	19
7.	Non Credit/Audit Course	✓	✓	00	00	
8.	**TOTAL CREDIT**	**23**	**21**	**19**	**12**	**75**

VL4153 GRAPH THEORY AND OPTIMIZATION TECHNIQUES L T P C
3 1 0 4

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in a real life situation.
- To provide knowledge and training using non-linear programming under limited resources for engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

UNIT I GRAPHS 12

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM 12

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING 12

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING 12

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- apply graph ideas is solving connectivity related problems.
- apply fundamental graph algorithms to solve certain optimization problems.
- formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- model various real life situations as optimization problems and effect their solution through Non-linear programming.
- apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

TEXT BOOKS:

1. Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, New Delhi, 2010.
2. Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012.

3. Sharma J.K., “Operation Research”, 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, “Introduction to Graph Theory”, Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., “ A text book of Graph Theory”, Springer Science and Business Media, New Delhi, 2012.
6. Narasingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, Prentice Hall India,1997.

RM4151 RESEARCH METHODOLOGY AND IPR L T P C
2 0 0 2

UNIT I RESEARCH DESIGN 6

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES 6

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING 6

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS 6

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS 6

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

VL4151 **ANALOG IC DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog IC will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER 9

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.

UNIT V BANDGAP REFERENCES 9

Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: Design amplifiers to meet user specifications
CO2: Analyse the frequency and noise performance of amplifiers
CO3: Design and analyse feedback amplifiers and one stage op amps
CO4: Design and analyse two stage op amps
CO5: Design and analyse current mirrors and current sinks with mos devices

TOTAL: 45 PERIODS

REFERENCES

1. Behzad Razavi, “Design Of Analog Cmos Integrated Circuits”, Tata Mcgraw Hill, 2001.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar And Mos Analog Integrated Circuit Design”, John Wiley & Sons,Inc.,2003.
4. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2nd Edition, 2002.
5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.

VL4152	DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES 6

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

CO2: Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort

CO3: Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches

CO4: Understand design methodology of arithmetic building blocks

CO5: Design functional units including ROM and SRAM

REFERENCES:

1. N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993
2. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998
4. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

AP4152 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 2 4

COURSE OBJECTIVES:

- To design asynchronous sequential circuits.
- To learn about hazards in asynchronous sequential circuits.
- To study the fault testing procedure for digital circuits.
- To understand the architecture of programmable devices.
- To design and implement digital circuits using programming tools.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Circuits and Modelling- State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards – Mixed Operating Mode Asynchronous Circuits – Designing Vending Machine Controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm –– Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes – Built in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming Logic Device Families – Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA – Xilinx FPGA - Xilinx 4000.

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types And Operators For Modelling In Verilog HDL - Behavioural Descriptions In Verilog HDL – HDL Based Synthesis – Synthesis Of Finite State Machines– Structural Modelling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters – Sequential Machine – Serial Adder – Multiplier- Divider – Design Of Simple Microprocessor, Introduction To System Verilog.

45 PERIODS

SUGGESTED ACTIVITIES:

1: Design asynchronous sequential circuits.
2: Design synchronous sequential circuits using PLA/PAL.
3: Simulation of digital circuits in FPGA.
4: Design digital systems with System Verilog.

PRACTICAL EXERCISES: 30 PERIODS

1. Design of Registers by Verilog HDL.
2. Design of Counters by Verilog HDL.
3. Design of Sequential Machines by Verilog HDL.
4. Design of Serial Adders , Multiplier and Divider by Verilog HDL.
5. Design of a simple Microprocessor by Verilog HDL.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Analyse and design synchronous sequential circuits.
CO2: Analyse hazards and design asynchronous sequential circuits.
CO3: Knowledge on the testing procedure for combinational circuit and PLA.
CO4: Able to design PLD and ROM.
CO5: Design and use programming tools for implementing digital circuits of industry standards.

TOTAL:75 PERIODS

REFERENCES:

1. Charles H.Roth jr., “Fundamentals of Logic Design” Thomson Learning,2013.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001.
5. Paragk.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
6. Paragk.Lala “Digital System Design Using PLD” B S Publications,2003.
7. Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

AP4153 SEMICONDUCTOR DEVICES AND MODELING L T P C

3 0 0 3

COURSE OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theory and devices and their applications.
- To gain adequate understanding of semiconductor device modelling aspects, designing devices for electronic applications

- To acquire the fundamental knowledge of different semiconductor device modelling aspects.

UNIT I MOS CAPACITORS 9

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Nonequilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–OxideInterface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II MOSFET DEVICES 9

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III CMOS DEVICE DESIGN 9

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV BIPOLAR DEVICES 9

n–p–n Transistors, Basic Operation of a Bipolar Transistor, Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Collector Current, Base Current, Current Gains, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Nonideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.

UNIT V MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, the students will be able to

CO1: Explore the properties of MOS capacitors.

CO2: Analyze the various characteristics of MOSFET devices.

CO3: Describe the various CMOS design parameters and their impact on performance of the device.
CO4: Discuss the device level characteristics of BJT transistors.
CO5: Identify the suitable mathematical technique for simulation.

REFERENCES:

1. Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.
2. A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd, 2009.
3. Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009
4. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004
5. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
6. Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition, 2014
7. J P Collinge, C A Collinge, “Physics of Semiconductor devices” Springer, 2002.
8. S.M.Sze, Kwok.K. NG, “Physics of Semiconductor devices”, Springer, 2006.

VL4111	FPGA LABORATORY	L	T	P	C
		0	0	4	2

COURSE OBJECTIVES:

- To help engineers read, understand, and maintain digital hardware models and conventional verification test benches written in Verilog and System Verilog.
- To provide a critical language foundation for more advanced training on System Verilog

LIST OF EXPERIMENTS

1. Introduction to Verilog and System Verilog
2. Running simulator and debug tools
3. Experiment with 2 state and 4 state data types
4. Experiment with blocking and non-blocking assignments
5. Model and verify simple ALU
6. Model and verify an Instruction stack
7. Use an interface between testbench and DUT
8. Developing a test program
9. Create a simple and advanced OO testbench
10. Create a scoreboard using dynamic array
11. Use mailboxes for verification
12. Generate constrained random test values
13. Using coverage with constrained random tests

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Understand and use the System Verilog RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy and connectivity features, and interfaces.

CO2: Appreciate and apply the System Verilog verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification.
CO3: The implementation of higher level of abstraction to design and verification
CO4: Develop Verilog test environments of significant capability and complexity.
CO5: Integrate scoreboards, multichannel sequencers and Register Models

VL4112 ANALOG IC DESIGN LABORATORY L T P C
0 0 4 2

COURSE OBJECTIVES:

- Carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, exposure to state of art CAD VLSI tool in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

LIST OF EXPERIMENTS

1. Extraction of process parameters of CMOS process transistors
   a. Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS.
   b. Plot I_D vs. V_{GS} at particular drain voltage for NMOS, PMOS and determine Vt.
   c. Plot log I_D vs. VGS at particular gate voltage for NMOS, PMOS and determine I_{OFF} and sub-threshold slope.
   d. Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   e. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use V_{DS} of appropriate voltage To extract V_{th} use the following procedure.
      i. Plot g_m vs V_{GS} using SPICE and obtain peak g_m point.
      ii. Plot $y=I_D/(g_m)$ as a function of VGS using SPICE.
      iii. Use SPICE to plot tangent line passing through peak gm point in y (V_{GS}) plane and determine V_{th}.
   f. Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it.

2. CMOS inverter design and performance analysis
   a. i. Plot VTC curve for CMOS inverter and thereon plot dV_{out} vs. dV_{in} and determine transition voltage and gain g. Calculate V_{IL}, V_{IH}, NM_H, NM_L for the inverter.
   ii. Plot VTC for CMOS inverter with varying V_{DD}.
   iii. Plot VTC for CMOS inverter with varying device ratio.
   b. Perform transient analysis of CMOS inverter with no load and with load and determine propagation delay t_{pHL}, t_{pLH}, 20%-to-80% rise time t_r and 80%-to-20% fall time t_f.
   c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis

a. Plot small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors.
b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
   i. Establish a test bench to achieve $V_{DSQ}=V_{DD}/2$.
   ii. Calculate input bias voltage for a given bias current.
   iii. Use spice and obtain the bias current. Compare with the theoretical value
   iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier
   v. using small signal analysis in spice, considering load capacitance.
   vi. Plot step response of the amplifier with a specific input pulse amplitude.
   vii. Derive time constant of the output and compare it with the time constant
   viii. resulted from -3dB Band Width.
   ix. Use spice to determine input voltage range of the amplifier

5. Three OPAMP Instrumentation Amplifier (INA).
Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
   i. Draw the schematic of op-amp macro model.
   ii. Draw the schematic of INA.
   iii. Obtain parameters of the op-amp macro model such that it meets a given specification for:
   i.low-frequency voltage gain,
   ii.unity gain BW (fu),
   iii.input capacitance,
   iv.output resistance,
   v.CMRR

d. Draw schematic diagram of CMRR simulation setup.
e. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
f. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
g. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting.

6. Use Layout editor.
a. Draw layout of a minimum size inverter using transistors from CMOS process library. Use Metal 1 as interconnect line between inverters.
b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.
c. Extract the netlist. Use extracted netlist and obtain $t_{PHL}t_{PLH}$ for the inverter using Spice.
d. Use a specific interconnect length and connect and connect three inverters in a chain.
e. Extract the new netlist and obtain t_{PHL} and t_{PLH} of the middle inverter.
f. Compare new values of delay times with corresponding values obtained in part ‘c’.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
   a. low-frequency voltage gain,

b. unity gain BW (fu),
c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.
ii. Perform time domain simulation and verify low frequency gain.
iii. Perform AC analysis and verify.

TOTAL: 60 PERIODS

COURSE OUTCOMES:
On successful completion of this course, students will be able to
CO1: Design digital and analog Circuit using CMOS given a design specification.
CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances
CO3: Use EDA tools for Circuit Design

VL4251 DESIGN FOR VERIFICATION USING UVM L T P C
3 0 0 3

COURSE OBJECTIVES:

- To provide the students complete understanding on UVM testing
- To become proficient at UVM verification,
- To provide an experience on self checking UVM testbenches

UNIT I INTRODUCTION 9
Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation

UNIT II DEVELOPING REUSABLE VERIFICATION COMPONENTS 9
Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage

UNIT III UVM USING VERIFICATION COMPONENTS 9
Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes -Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model

UNIT IV UVM USING THE REGISTER LAYER CLASSES 9
Using The Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register- Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences

UNIT V ASSIGNMENT IN TESTBENCHES 9
Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

CO1:understand the basic concepts of two methodologies UVM

CO2:build actual verification components.

CO3:generate the register layer classes.

CO4:code testbenches using UVM.

CO5:understand advanced peripheral bus testbenches.

REFERENCES

1. The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi, 2013.
2. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Greg Tumbush, 3rd edition, 2012.
3. https://www.udemy.com/learn-ovm-UVM/ 2.
4. http://www.testbench.in/ut_00_index.html 3.
5. http://www.testbench.in/ot_00_index.html
6. https://www.accellera.org/images/downloads/standards/UVM/UVM_users_guide_1.2.pdf

VL4291 LOW POWER VLSI DESIGN L T P C

3 0 0 3

COURSE OBJECTIVES:

- identify sources of power in an IC.
- identify the power reduction techniques based on technology independent and technology dependent methods
- identify suitable techniques to reduce the power dissipation
- estimate power dissipation of various MOS logic circuits
- develop algorithms for low power dissipation

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of Limits of Power – Sources of Power Consumption – Physics of Power Dissipation in CMOS FET Devices – Basic Principle of Low Power Design.

UNIT II POWER OPTIMIZATION 9

Logic Level Power Optimization – Circuit Level Low Power Design – Gate Level Low Power Design –Architecture Level Low Power Design – VLSI Subsystem Design of Adders, Multipliers, PLL, Low Power Design

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer Arithmetic Techniques for Low Power System – Reducing Power Consumption in Combinational Logic, Sequential Logic, Memories – Low Power Clock – Advanced Techniques – Special Techniques, Adiabatic Techniques – Physical Design, Floor Planning, Placement and Routing.

UNIT IV POWER ESTIMATION 9

Power Estimation Techniques, Circuit Level, Gate Level, Architecture Level, Behavioral Level, – Logic Power Estimation – Simulation Power Analysis –Probabilistic Power Analysis

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER CMOS CIRCUITS 9

Synthesis for Low Power – Behavioral Level Transform –Algorithms for Low Power – Software Design for Low Power.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: able to find the power dissipation of MOS circuits

CO2: design and analyze various MOS logic circuits

CO3 :apply low power techniques for low power dissipation

CO4: able to estimate the power dissipation of ICs

CO5: able to develop algorithms to reduce power dissipation by software.

REFERENCES

1. Kaushik Roy and S.C.Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley, 2000
2. J.B.Kulo and J.H Lou, “Low Voltage CMOS VLSI Circuits”, Wiley 1999.
3. James B.Kulo, Shih-Chia Lin, “Low Voltage SOI CMOS VLSI Devices and Circuits”, John Wiley and Sons, Inc. 2001
4. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009

VL4292 RFIC DESIGN L T P C

3 0 0 3

COURSE OBJECTIVES:

- to study the various impedance matching techniques used in RF circuit design.
- to understand the functional design aspects of LNAs, Mixers, PLLs and VCOs.
- to understand frequency synthesis.

UNIT I IMPEDANCE MATCHING IN AMPLIFIERS 9

Definition of ‘Q’, Series Parallel Transformations of Lossy Circuits, Impedance Matching Using ‘L’, ‘Pi’ and T Networks, Integrated Inductors, Resistors, Capacitors, Tunable Inductors, Transformers

UNIT II AMPLIFIER DESIGN 9

Noise Characteristics of MOS Devices, Design of CG LNA and Inductor Degenerated LNAs. Principles of RF Power Amplifiers Design

UNIT III ACTIVE AND PASSIVE MIXERS 9

Qualitative Description of the Gilbert Mixer - Conversion Gain, and Distortion and Noise , Analysis of Gilbert Mixer – Switching Mixer - Distortion in Unbalanced Switching Mixer -Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - a Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV OSCILLATORS 9

LC Oscillators, Voltage Controlled Oscillators, Ring Oscillators, Delay Cells, Tuning Range in Ring Oscillators, Tuning in LC Oscillators, Tuning Sensitivity, Phase Noise in Oscillators, Sources of Phase Noise

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Phase Detector/Charge Pump, Analog Phase Detectors, Digital Phase Detectors, Frequency Dividers, Loop Filter Design, Phase Locked Loops, Phase Noise in PLL, Loop Bandwidth, Basic Integer-N Frequency Synthesizer, Basic Fractional-N Frequency Synthesizer

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: to understand the principles of operation of an RF receiver front end

CO2: to design and apply constraints for LNAs, Mixers and frequency synthesizers

CO3: to analyze and design mixers

CO4: to design different types of oscillators and perform noise analysis

CO5: to design PLL and frequency synthesizer

REFERENCES

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mcgraw-Hill, 1999
4. Jia-Sheng Hong, "Microstrip Filters for RF/Microwave Applications", Wiley, 2001
5. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003

VL4252 VLSI TESTING L T P C

3 0 0 3

COURSE OBJECTIVES:

- to introduce the VLSI testing.
- to introduce logic and fault simulation and testability measures
- to study the test generation for combinational and sequential circuits
- to study the design for testability.
- to study the fault diagnosis

UNIT I INTRODUCTION TO TESTING 9

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship Among Fault Models.

UNIT II LOGIC & FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS 9

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG

UNIT IV DESIGN FOR TESTABILITY 9

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built-in Self-Test – Random Logic Bist – DFT for Other Test Objectives.

UNIT V FAULT DIAGNOSIS 9

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Understand VLSI Testing Process
CO2: Develop Logic Simulation and Fault Simulation
CO3:Develop Test for Combinational and Sequential Circuits
CO4: Understand the Design for Testability
CO5:Perform Fault Diagnosis.

REFERENCES

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017
2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

VL4211 VERIFICATION USING UVM LABORATORY

L	T	P	C
0	0	4	2

COURSE OBJECTIVES:

- to help the engineers to design the system with verilog and system Verilog
- Complete understanding of Verilog Hardware Description Language
- to practice for writing synthesizable RTL models that work correctly in both simulation and synthesis.

LIST OF EXPERIMENTS

1. Simulate a simple UVM testbench and DUT
2. Examining the UVM testbench
3. Design and simulate sequence items and sequence
4. Design and simulate a UVM driver and sequencer

5. Design and simulating UVM monitor and agent
6. Design, simulate and examine coverage
7. Design and simulate a UVM scoreboard and environment, and verifying the outputs of a (faulty) DUT
8. Design and simulate a test that runs multiple sequence
9. Design and simulate a configurable UVM test environment

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: understand the features and capabilities of the UVM class library for system Verilog

CO2: combine multiple UVCs into a complete verification environment

CO3:create and configure reusable, scalable, and robust UVM verification components (UVCs)

CO4: create a UVM testbench structure using the UVM library base classes and the UVM factory

CO5:develop a register model for your DUT and use the model for initialization and accessing DUT registers

VL4212 TERM PAPER WRITING AND SEMINAR L T P C

0 0 2 1

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (atleast 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the authors contributions and critically analysing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained.

Activities to be carried out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Stating an Objective			

Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered	4th week	**6%** (the list of standard papers and reason for selection)
Reading and notes for first 5 papers	• Reading Paper Process • For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's	5th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)

	work, in the author's opinion? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? • Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next5 papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%** (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and

			classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%** (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	**10%** (based on presentation and Viva-voce)

TOTAL: 30 PERIODS

VL4351 VLSI SIGNAL PROCESSING **L T P C 3 0 0 3**

COURSE OBJECTIVES:

- to introduce techniques for altering existing DSP structures to suit VLSI implementations.
- to introduce efficient design of DSP architectures suitable for VLSI.

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS **9**

Introduction to DSP systems – typical DSP algorithms, data flow and dependence graphs - critical path, loop bound, iteration bound, longest path matrix algorithm, pipelining and parallel processing of FIR filters, pipelining and parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION **9**

Retiming – definitions and properties, unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even, Merge-Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS **9**

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – advanced techniques – special techniques, adiabatic techniques – physical design, floor planning, placement and routing.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES **9**

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, design of lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS WAVE AND ASYNCHRONOUS PIPELINING **9**

Numerical strength reduction – sub-expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining - Bundled Data versus Dual-Rail protocol.

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: Ability to determine the parameters influencing the efficiency of DSP architectures and apply pipelining and parallel processing techniques to alter FIR structures for efficiency

CO2: Ability to analyse and modify the design equations leading to efficient DSP architectures for transforms apply low power techniques for low power dissipation

CO3: Ability to speed up convolution process and develop fast and area efficient IIR structures

CO4: Ability to develop fast and area efficient multiplier architectures

CO5: Ability to reduce multiplications and build fast hardware for synchronous digital systems

REFERENCES

1. Keshab K. Parhi, “ VLSI Digital Signal Processing Systems, Design and Implementation “, Wiley, Interscience, 2007
2. U. Meyer – Baese, “ Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2nd Edition, 2004.

VL4071 ASIC DESIGN **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To Focus on the Semi-Custom IC Design and introduces the Principles of Design Logic Cells, I/O Cells and Interconnect Architecture, with Equal Importance given to FPGA and ASIC styles.
- To deal with the entire FPGA and ASIC Design Flow from the Circuit and Layout Design Point of View

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN **9**

Types of Asics - Design Flow - CMOS Transistors - Combinational Logic Cell – Sequential Logic Cell - Data Path Logic Cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical Effort.

UNIT II **PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS** **9**

Anti Fuse - Static Ram - EPROM and EEPROM Technology - ACTEL ACT- Xilinx LCA –ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.

UNIT III **PROGRAMMABLE ASIC ARCHITECTURE** **9**

Architecture and Configuration of ARTIX / Cyclone and KINTEX Ultra Scale / STRATIX FPGA – Micro-Blaze / NIOS Based Embedded Systems – Signal Probing Techniques.

UNIT IV **LOGIC SYNTHESIS, PLACEMENT AND ROUTING** **9**

Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

UNIT V **SYSTEM-ON-CHIP DESIGN** **9**

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators. Case Studies: Digital Camera, SDRAM, High Speed Data standards.

TOTAL :45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be

CO1: able to apply Logical Effort Technique for predicting Delay, Delay Minimization and FPGA Architectures

CO2: able to Design Logic Cells and I/O Cells

CO3: able to analyze the various resources of recent FPGAs

CO4: able to use Algorithms for Floor Planning and Placement of Cells and to Apply Routing Algorithms for Optimization of Length and Speed.

CO5: able to analyze High Performance Algorithms Available for ASICs

REFERENCES

1. M.J.S.Smith, "Application Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science,2006
3. Roger Woods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, “FPGA-Based Implementation of Signal Processing Systems”, Wiley, 2008.

VE4152 **EMBEDDED SYSTEM DESIGN** **L T P C**

3 0 0 3

COURSE OBJECTIVES:

- To understand the design challenges in embedded systems.
- To program the Application Specific Instruction Set Processors.
- To understand the bus structures and protocols.
- To model processes using a state – machine model.
- To design a real time embedded system.

UNIT I EMBEDDED SYSTEM OVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES 9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS 9

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.

UNIT V SYSTEM DESIGN 9

Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

SUGGESTED ACTIVITIES:

1: Do microcontroller based design experiments.
2: Create program –state models for different embedded applications.
3: Design and develop embedded solutions for real world problems.

COURSE OUTCOMES:

CO1: Knowledge of different protocols
CO2: Apply state machine techniques and design process models.
CO3: Apply knowledge of embedded sotware development tools and RTOS
CO4: Apply networking principles in embedded devices.
CO5: Design suitable embedded systems for real world applications.

TOTAL:45 PERIODS

REFERENCES:

1. Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & Sons, 2009.
2. Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004.
3. Bruce Powel Douglas, "Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 2004, Pearson Education
4. Daniel W.Lewis, "Fundamentals of Embedded Software where C and Assembly Meet", Pearson Education, 2004
5. Bruce Powel Douglas, "Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems", 3rd Edition 1999, Pearson Education.

EL4071 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C
3 0 0 3

COURSE OBJECTIVES:

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM) interference and compatibility
- To develop a theoretical understanding of electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand the need for standards and to appreciate measurement methods
- To understand how EMI impacts wireless and broadband technologies

UNIT I INTRODUCTION & SOURCES OF EM INTERFERENCE 9

Introduction - Classification of sources - Natural sources - Man-made sources - Survey of the electromagnetic environment.

UNIT II EM SHIELDING 9

Introduction - Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency, magnetic field shielding - Effects of apertures

UNIT III INTERFERENCE CONTROL TECHNIQUES 9

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.

UNIT IV EMC STANDARDS, MEASUREMENTS AND TESTING 9

Need for standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments.

UNIT V EMC CONSIDERATIONS IN WIRELESS AND BROADBAND TECHNOLOGIES 9

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.

SUGGESTED ACTIVITIES:

1. Investigate various case studies related to EMIC. Example: Chernobyl Disaster in 1986.
2. Develop some understanding about the design of EM shields in electronic system design and packaging.

COURSE OUTCOMES:

Upon completion of this course, the student will be able to

CO1: Demonstrate knowledge of the various sources of electromagnetic interference
CO2: Display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems based on that understanding
CO3: Explain the EMI mitigation techniques of shielding and grounding
CO4: Explain the need for standards and EMC measurement methods
CO5: Discuss the impact of EMC on wireless and broadband technologies

TOTAL:45 PERIODS

REFERENCES

1. Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press, Second Edition, Indian Edition, 2013.
2. Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition,2008.
3. Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,2010.
4. Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork,2009.
5. Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997.

VL4001 DATA CONVERTERS L T P C
3 0 0 3

COURSE OBJECTIVES:

- To teach Analog to Digital and Digital to Analog Converters characteristics
- To teach the design of Switched Capacitor based Circuits
- To teach the design of Analog to Digital and Digital to Analog Converters

UNIT I INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS 9

Evolution, Types and Applications of AD/DA Converter Characteristics, Issues in Sampling, Quantization and Reconstruction, Oversampling and Anti-aliasing Filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-Capacitor Amplifiers, Switched Capacitor Integrator, Switched Capacitor Common Mode Feedback. Single Stage Amplifier as Comparator, Cascaded Amplifier Stages as Comparator, Latched Comparators. Offset Cancellation, Op Amp Offset Cancellation, Calibration Techniques

UNIT III NYQUIST RATE D/A CONVERTERS 9

Current Steering DACs, Capacitive DACs, Binary Weighted Vs. Thermometer DACS, Issues in Current Element Matching, Clock Feed Through, Zero Order Hold Circuits, DNL, INL and Other Performance Metrics of ADCs and DACs

UNIT IV PIPELINE AND OTHER ADCS 9

Performance Metrics, Flash Architecture, Pipelined Architecture, Successive Approximation Architecture, Time Interleaved Architecture.

UNIT V SIGMA DELTA CONVERTERS 9

STF, NTF, First Order and Second Order Sigma Delta Modulator Characteristics, Estimating The Maximum Stable Amplitude, CTDSMs, Op amp Nonlinearities

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be

CO1:able to carry out the design calculations for developing the various blocks associated with a typical CMOS AD or DA Converter.

CO2: able to design and implement circuits using Switched Capacitor Concepts

CO3: able to analyze and design D/A Converters

CO4: able to design different types of A/Ds

CO5: able to analyze and design Sigma Delta converter

REFERENCES

1. Behzad Razavi, “Principles of Data Conversion System Design”, IEEE Press, 1995.
2. M. Pelgrom, “Analog-to-Digital Conversion”, Springer, 2010.
3. Rudy Van De Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Acedamic Publishers, Boston, 2003.
4. J. G. Proakis, D. G. Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Prentice Hall, 4th Edition, 2006.
5. Shanthi Pavan, Richard Schreier, Gabor C. Temes , “Understanding Delta-Sigma Data Converters”, Willey –IEEE Press, 2nd Edition, 2017.

VL4002	HARDWARE SOFTWARE CO-DESIGN FOR FPGA	L T P C 3 0 0 3

COURSE OBJECTIVES:

- To acquire the knowledge about system specification and modelling
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Processor Architectures with One ASIC, Single-Processor Architectures with Many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-Simulation

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to

CO1: Describe The Broad Range of System Architectures and Design Methodologies that currently exist and define their fundamental attributes.

CO2: Discuss the Dataflow Models as a State-of-the-Art Methodology to Solve Co-Design Problems and to Optimize the balance between Software and Hardware.

CO3: Understand in Translating between Software and Hardware Descriptions through Co-Design Methodologies.

CO4: Understand the State-of-The-Art practices in developing Co-Design Solutions to problems using modern Hardware/Software Tools for building prototypes.

CO5: Understand the Concurrent Specification from an Algorithm, Analyze its behavior and partition the Specification into Software (C Code) and Hardware (HDL) Components

REFERENCES

1. Patrick Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer,2010.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Publisher, 1998.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Publisher,1997.
4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design”, Kaufmann Publisher,2001.

IF4094 PATTERN RECOGNITION L T P C

3 0 0 3

COURSE OBJECTIVES:

- Understand the in-depth concept of Pattern Recognition
- Implement Bayes Decision Theory
- Understand the in-depth concept of Perception and related Concepts
- Understand the concept of ML Pattern Classification
- Understand the concept of DL Pattern Recognition

UNIT I PATTERN RECOGNITION 8

Induction Algorithms. Rule Induction. Decision Trees. BayesianMethods. Overview. NaiveBayes. The Basic Na¨ıve Bayes Classifier. Naive Bayes Induction for Numeric Attributes. Correction to the

Probability Estimation. Laplace Correction. No Match. Other Bayesian Methods. Other Induction Methods. Neural Networks. Genetic Algorithms. Instance-based Learning. Support Vector Machines.

UNIT II STATISTICAL PATTERN RECOGNITION 8

About Statistical Pattern Recognition. Classification and regression. Features, Feature Vectors, and Classifiers. Pre-processing and feature extraction. The curse of dimensionality. Polynomial curve fitting. Model complexity. Multivariate non-linear functions. Bayes' theorem. Decision boundaries. Parametric methods. Sequential parameter estimation. Linear discriminant functions. Fisher's linear discriminant. Feed-forward network mappings.

UNIT III BAYES DECISION THEORY CLASSIFIERS 11

Bayes Decision Theory. Discriminant Functions and Decision Surfaces. The Gaussian Probability Density Function. The Bayesian Classifier for Normally Distributed Classes. Exact interpolation. Radial basis function networks. Network training. Regularization theory. Noisy interpolation theory. Relation to kernel regression. Radial basis function networks for classification. Comparison with the multi-layer perceptron. Basis function optimization.

UNIT IV LINEAR DISCRIMINANT FUNCTIONS 9

Linear Discriminant Functions and Decision Surfaces. The Two-Category Case. The Multicategory Case. The Perceptron Criterion Function. Batch Perceptron. Perceptron Algorithm Convergence. The Pocket Algorithm. Mean Square Error Estimation. Stochastic Approximation and the LMS Algorithm. Convergence Proof for Single-Sample Correction. Fixed increment descent. Some Direct Generalizations. Fixed increment descent. Batch variable increment Perceptron. Balanced Winnow algorithm. Relaxation Procedures. The Descent Algorithm

UNIT V NONLINEAR CLASSIFIERS 9

The Two Layer Perception. The Three Layer Perception. Algorithms Based On Exact Classification Of The Training Set. Feedforward operation and classification. General feedforward operation. Expressive power of multilayer networks. Backpropagation algorithm. Network learning. Training protocols. Stochastic Backpropagation. Batch Backpropagation. Radial basis function networks (RBF). Special bases. Time delay neural networks (TDNN). Recurrent networks. Counter propagation. Cascade-Correlation. Cascade-correlation. Neocognitron

TOTAL : 45 PERIODS

SUGGESTED ACTIVITIES:

1: Car Sales Pattern Classification using Support Vector Classifier
2: Avocado Sales Pattern Recognition using Linear regression
3: Tracking Movements by implementing Pattern Recognition
4: Detecting Lanes by implementing Pattern Recognition
5: Pattern Detection in SAR Images

COURSE OUTCOMES:

CO1: Discover imaging, and interpretation of temporal patterns
CO2: Identify Structural Data Patterns
CO3: Implement Pattern Classification using Machine Learning Classifiers
CO4: Implement Pattern Recognition using Deep Learning Models
CO5: Implement Image Pattern Recognition

REFERENCES

1. Pattern Classification, 2nd Edition, Richard O. Duda, Peter E. Hart, and David G. Stork.

Wiley, 2000
2. Pattern Recognition, Jürgen Beyerer, Matthias Richter, and Matthias Nagel. 2018
3. Pattern Recognition and Machine Learning, Christopher M. Bishop. Springer, 2010
4. Pattern Recognition and Classification, Dougherty, and Geoff. Springer, 2013
5. Practical Machine Learning and Image Processing, Himanshu Singh. Apress, 2019

VL4003 DSP STRUCTURES FOR VLSI L T P C
3 0 0 3

COURSE OBJECTIVES:

- to understand the fundamentals of DSP
- to learn various DSP structures and their implementation.
- to know designing constraints of various filters
- design and optimize VLSI architectures for basic DSP algorithms
- to enable students to design VLSI system with high speed and low power.
-

UNIT I INTRODUCTION TO DIGITAL SIGNAL PROCESSING 9

Linear system theory- convolution- correlation - DFT- FFT- basic concepts in FIR filters and IIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-DFG.

UNIT II ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER 9

Data-flow graph representations- Loop bound and Iteration bound algorithms for computing iteration bound-LPM algorithm. Pipelining and parallel processing: pipelining of FIR digital filters-parallel processing, pipelining and parallel processing for low power.

UNIT III RETIMING, UNFOLDING AND FOLDING 9

Retiming: definitions, properties and problems- solving systems of inequalities. Properties of Unfolding, critical path, Unfolding and Retiming, applications of Unfolding, Folding transformation-register minimization techniques, register minimization in folded architecture- folding of multirate system.

UNIT IV FAST CONVOLUTION 9

Cook-toom algorithm- modified cook-Toom algorithm. Design of fast convolution algorithm by inspection - Winograd algorithm- modified Winograd algorithm

UNIT V ARITHMETIC STRENGTH REDUCTION IN FILTERS 9

Parallel FIR filters-fast FIR algorithms-two parallel and three parallel. Parallel architectures for rank order filters -odd-even, merge-sort architecture-rank order filter architecture-parallel rank order filters-running order merge order sorter, low power rank order filter.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course student will be able

CO1: acquired knowledge about fundamentals of DSP processors.

CO2: improve the overall performance of DSP system through various transformation and optimization techniques.

CO3: to understand the need of different types of instructions for DSP.

CO4: optimize design in terms of computation complexity and speed.

CO5: understand clock based issues and design asynchronous and wave pipelined systems**.**

REFERENCES

1. K.K Parhi: "VLSI Digital Signal Processing", John-Wiley, 2nd Edition Reprint, 2008.
2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009.

VL4004 POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS L T P C
3 0 0 3

COURSE OBJECTIVES:

- to design ~~of~~ reference circuits and low dropout regulators for desired specifications
- to understand oscillators choice and requirements for clock generation circuits
- to design clock generation and recovery in the context of high speed systems

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current mirrors, self biased current reference, startup circuits, VBE based current reference, VT based current reference, band gap reference , supply independent biasing, temperature independent biasing, PTAT current generation, constant Gm biasing.

UNIT II LOW DROP OUT REGULATORS 9

Analog building blocks, negative feedback, performance metrics, AC design, stability, internal and external compensation, PSRR – internal and external compensation circuits

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, ring oscillators, LC oscillators, Colpitts oscillator, jitter and phase noise in ring oscillators, impulse sensitivity function for LC & ring oscillators, phase noise in differential LC oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS 9

PLL fundamental, PLL stability, noise performance, charge-pump PLL topology, CPPLL building blocks, jitter and phase noise performance, DLL fundamentals.

UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

CDR architectures, transimpedance amplifiers and limiters, CMOS interface, linear half rate CMOS CDR circuits, wide capture range CDR circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1:design band gap reference circuits and low drop out regulator for a given specification.

CO2: understand specification related to supply and clock generation circuits of IC

CO3: choose oscillator topology and design meeting the requirement of clock generation circuits.

CO4: design clock generation circuits in the context of high speed I/Os, high speed broad band communication circuits and data conversion circuits.

CO5: Design clock distribution circuits

REFERENCES

1. Gabriel.a. Rincon-Mora, "Voltage References from Diode to Precision Higher Order Band gap circuits", John Wiley & Sons Inc, 2002.
2. Gabriel.a. Rincon-Mora, "Analog IC Design with Low-Dropout Regulators", Mcgraw-Hill Professional Pub, 2009.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mcgraw Hill, 2001
4. Floyd M. Gardner ,"Phase Lock Techniques" John Wiley& Sons, Inc 2005.
5. Michiel Steyaert, Arthur H.M. Van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-Performance Amplifiers Power Management", Springer, 2008.
6. Behzadrazavi, "Design of Integrated Circuits for Optical Communications", McGraw Hill, 2003.

VL4005 RECONFIGURABLE ARCHITECTURES L T P C

3 0 0 3

COURSE OBJECTIVES:

- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processors
- to learn the concepts of implementation, synthesis and placement of modules in reconfigurable architectures
- to understand the communication techniques and System on Programmable Chip for reconfigurable architectures
- to learn the process of reconfiguration management
- to familiarize the applications of reconfigurable architectures

UNIT - I INTRODUCTION 9

General purpose computing – domain specific processors – Application Specific Processors – reconfigurable computing – fields of application – evolution of reconfigurable systems – simple Programmable Logic Devices – Complex Programmable Logic Devices – Field Programmable Gate Arrays – coarse grained reconfigurable devices.

UNIT - II IMPLEMENTATION, SYNTHESIS AND PLACEMENT 9

Integration – FPGA design flow – logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device's free and occupied spaces.

UNIT – III COMMUNICATION AND SOPC 9

Direct communication – communication over third party – bus based communication – circuit switching – Network on Chip – dynamic Network on Chip – System on a Programmable Chip – adaptive multi-processing on chip.

UNIT – IV RECONFIGURATION MANAGEMENT 9

Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.

UNIT – V APPLICATIONS 9

FPGA based parallel pattern matching - low power FPGA based architecture for microphone arrays in Wireless Sensor Networks - exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems.

TOTAL :45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: analyze the different architecture principles relevant to reconfigurable computing systems
CO2: compare the tradeoffs that are necessary to meet the area, power and timing criteria of reconfigurable systems
CO3: analyze the algorithms related to placement and partitioning
CO4:analyze the communication techniques and system on programmable chip for reconfigurable architectures
CO5: analyze the principles of Network and System on a Programmable Chip

REFERENCES

1. Christophe Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer 2007.
2. Scott Hauck and Andre Dehon, “Reconfigurable Computing: The Theory and Practice of FPGA Based Computation”, Elsevier 2008
3. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
4. Nikoloas Voros Et Al. “Applied Reconfigurable Computing: Architectures, Tools and Applications” Springer, 2018.
5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, “Reconfigurable Computing: Architectures and Applications”, Springer 2006.

VL4006 ADVANCED WIRELESS SENSOR NETWORKS L T P C
3 0 0 3

COURSE OBJECTIVES:

- to enable the student to understand the role of sensors and the networking of sensed data for different applications.
- to expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- to enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for wireless sensor networks-characteristics requirements-required mechanisms, difference between mobile ad-hoc and sensor networks, applications of sensor networks- case study, enabling technologies for wireless sensor networks.

UNIT II ARCHITECTURES 9

Single-node architecture - hardware components, energy consumption of sensor nodes , operating systems and execution environments, network architecture - sensor network scenarios, optimization goals and figures of merit, gateway concepts. Physical layer and transceiver design considerations.

UNIT III MAC AND ROUTING 9

MAC protocols for wireless sensor networks, IEEE 802.15.4, Zigbee, low duty cycle protocols and wakeup concepts - s-MAC , the mediation device protocol, wakeup radio concepts, address and name management, assignment of MAC addresses, routing protocols- energy- efficient routing, geographic routing.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology control, clustering, time synchronization, localization and positioning, sensor tasking and control.

UNIT V DATA MANAGEMENT AND SECURITY 9

Data management in WSN, storage and indexing in sensor networks, query processing in sensor, data aggregation, directed diffusion, tiny aggregation, greedy aggregation, security in WSN, security protocols for sensor networks, secure charging and rewarding scheme, secure event and event boundary detection.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: design and implement simple wireless network concepts
CO2: design, analyze and implement different network architectures
CO3: implement MAC layer and routing protocols
CO4: deal with timing and control issues in wireless sensor networks
CO5: analyze and design secured wireless sensor networks

REFERENCES

1. Holger Karl & Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks" , John Wiley, 2005.

2. Erdal Çayirci , Chunming Rong, “Security in Wireless Ad Hoc and Sensor Networks”, John Wiley and Sons, 2009.
3. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-S Technology, Protocols, and Applications”, John Wiley, 2007.
4. Yingshu Li, My T. Thai,Weili Wu, “Wireless Sensor Networks and Applications”, Springer, 2008.

AP4095 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

COURSE OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to
CO1: identify sources affecting the speed of digital circuits.
CO2:identify methods to improve the signal transmission characteristics
CO3: characterise and model multiconductor transmission line

CO4: analyse clock distribution system and understand its design parameters
CO5: analyse nonideal effects of transmission line

REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall PTR , 2003.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handboo of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. **SPECTRAQUEST** from Cadence, http://www.specctraquest.com **or any equivalent open source tool**

II4092 SYSTEM ON CHIP L T P C
3 0 0 3

COURSE OBJECTIVE:

- To introduce architecture and design concepts underlying system on chips.
- Students can gain knowledge of designing SoCs.
- To impart knowledge about the hardware-software design of a modest complexity chip allthe way from specifications, modeling, synthesis and physical design.

UNIT I SYSTEM ARCHITECTURE: OVERVIEW 9

Components of the system – Processor architectures – Memory and addressing – system levelinterconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT II PROCESSOR SELECTION FOR SOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT III MEMORY DESIGN 9

SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and Dcaches – multilevel caches – SoC memory systems – board based memory systems – simpleprocessor/memory interaction.

UNIT IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, CoreConnect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices -

FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT V FPGA BASED EMBEDDED PROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors andHard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL:45 PERIODS

COURSE OUTCOMES:

Upon successful completion of the program the students shall

CO1: Explain all important components of a System-on-Chip and an embedded system, i.e.
CO2: digital hardware and embedded software;
CO3: Outline the major design flows for digital hardware and embedded software;
CO4: Discuss the major architectures and trade-offs concerning performance, cost and power
CO5: consumption of single chip and embedded systems;

REFERENCES:

1. Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008.
2. Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008

VL4073 MEMS AND NEMS L T P C
3 0 0 3

COURSE OBJECTIVES:

- to introduce the concepts of Micro Electro Mechanical devices.
- to know the fabrication process of microsystems.
- to know the design concepts of micro sensors and micro actuators.
- to familiarize concepts of Quantum Mechanics and Nano systems.

UNIT I OVERVIEW 9

New trends in Engineering and Science: Micro and Nanoscale systems, introduction to design of MEMS and NEMS, MEMS and NEMS – applications, devices and structures. Materials for MEMS: Silicon, Silicon compounds, polymers, metals

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem Fabrication Processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin Film Depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching Techniques: Dry and Wet Etching, Electrochemical Etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-Like) Technology; Packaging: Microsystems Packaging, Essential Packaging Technologies, Selection of Packaging Materials

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic Wave Sensors, Resonant Sensor, Vibratory Gyroscope, Capacitive and Piezo Resistive Pressure Sensors- Engineering Mechanics Behind These Microsensors. Case Study: Piezo-Resistive Pressure Sensor.

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation Using Thermal Forces, Actuation Using Shape Memory Alloys, Actuation Using Piezoelectric Crystals, Actuation using Electrostatic Forces (Parallel Plate, Torsion Bar, Comb Drive Actuators), Micromechanical Motors and Pumps. Case Study: Comb Drive Actuators.

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave Function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their Quantization, Molecular Wires and Molecular Circuits

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the student will be able to:

CO1: Discuss micro sensors
CO2: Explain micro actuators
CO3: Outline nanosystems and Quantum mechanics
CO4: Design micro actuators for different applications
CO5:Analyze atomic structures

REFERENCES

1. Chang Liu, “Foundations of MEMS”, Pearson Education India Limited, 2006.
2. Marc Madou, “Fundamentals of Microfabrication”, CRC Press 1997.
3. Stephen D. Senturia,” Micro System Design”, Kluwer Academic Publishers,2001
4. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press, 2002.
5. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.

VL4091 NETWORK ON CHIP L T P C

3 0 0 3

COURSE OBJECTIVES:

The students should be made to:

- Understand the concept of Network - on - Chip
- Learn router architecture designs
- Study fault tolerance Network - on – Chip

UNIT I INTRODUCTION TO NOC 9

Introduction to NOC – OSI Layer Rules in NOC - Interconnection Networks in Network-On-Chip Network Topologies - Switching Techniques - Routing Strategies - Flow Control Protocol Quality-of-Service Support

UNIT II ARCHITECTURE DESIGN 9

Switching Techniques and Packet Format - Asynchronous FIFO Design - GALS Style of Communication - Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design

UNIT III ROUTING ALGORITHM 9

Packet Routing-QOS, Congestion Control and Flow Control – Router Design – Network Link Design – Efficient and Deadlock-Free Tree-Based Multicast Routing Methods - Path-Based Multicast Routing For 2D and 3D Mesh Networks- Fault-Tolerant Routing Algorithms - Reliable and Adaptive Routing Algorithms

UNIT IV TEST AND FAULT TOLERANCE OF NOC 9

Design-Security in Networks-On-Chips-Formal Verification of Communications in Networks-On Chips-Test and Fault Tolerance For Networks-On-Chip Infrastructures-Monitoring Services For Networks-On-Chips

UNIT V THREE-DIMENSIONAL INTEGRATION OF NETWORK-ON-CHIP 9

Three-Dimensional Networks-On-Chips Architectures – A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures - Resource Allocation For QOS On-Chip Communication – Networks-On-Chip Protocols-On-Chip Processor Traffic Modeling For Networks-On-Chip

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Compare different architecture design

CO2: Discuss different routing algorithms

CO3: Explain three dimensional Networks on Chip architectures

CO4:Test and design fault tolerant NOC

CO5: Design three dimensional architectures of NOC

REFERENCES

1. ChrysostoMOSnicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-On - Chip " Architectures Holistic Design Exploration", Springer.
2. Fayezgebali, Haythamelmiligi, Hqhahedwatheq E1-Kharashi "Networks-On-Chips Theory and Practice CRC Press
3. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-On-Chip Architectures" 2013
4. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-On-Chip" 2014

CU4076 VLSI FOR WIRELESS COMMUNICATION L T P C

3 0 0 3

COURSE OBJECTIVES:

- To understand the concepts of basic wireless communication concepts.
- To study the parameters in receiver and low noise amplifier design.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of transmitters and power amplifiers in wireless

communication.

UNIT I COMMUNICATION CONCEPTS 9

Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading – Standard Translation.

UNIT II RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS 9

Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT III MIXERS 9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer. Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNIT IV FREQUENCY SYNTHESIZERS 9

PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider.

UNIT V TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS 9

Transmitter back end design – Quadrature LO generator – Power amplifier design.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

At the end of this course, the student should be able to

CO1: Able to recollect basic wireless communication concepts.

CO2: To understand the parameters in receiver and design a low noise amplifier

CO3: In a position to apply his knowledge on various types of mixers designed for wireless communication.

CO4: Design PLL and VCO

CO5: Understand the concepts of transmitters and utilize the power amplifiers in wireless communication.

TOTAL PERIODS:45

REFERENCES

1. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2002.
2. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,1998.
3. Behzad Razavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 1999.
4. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI wireless design – Circuits & Systems”, Kluwer Academic Publishers, 2000.
5. J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design,” Boston, Kluwer Academic Pub., 1997.
6. Thomas H.Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Cambridge University Press ,2003.

VL4074 **NANO TECHNOLOGY** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- Provides knowledge of various industrial applications of Nanotechnology
- Introduces the theory and practice on Nanomaterials
- Imparting the state of art of nanotechnology to the society and to the environmental implication
- To exercise the students' knowledge and imagination of Nanoscience and nanotechnology toward engineering applications coupled with detailed justifications.

UNIT I NANOTECHNOLOGY 9

Background, what is Nanotechnology, types of Nanotechnology and Nano-machines, top down and bottom up techniques, atomic manipulation-Nanodots, semi-conductor quantum dots, self-assembly monolayers, simple details of characterization tools- SEM, TEM, STM, AFM.

UNIT II NANOMATERIALS 9

What are Nanomaterials? Preparation of Nanomaterials- solid state reaction method, Chemical Vapor Deposition, SOL-GELS techniques, electrodeposition, ball milling, introduction to lithography, Pulse Laser Deposition (PLD), applications of Nanomaterials

UNIT III CARBON TUBES 9

New forms of carbon, carbon tubes-types of Nanotubes, formation of Nanotubes, assemblies, purification of carbon Nanotubes, properties of Nanotubes, applications of Nanotubes

UNIT IV OPTICS, PHOTONICS AND SOLAR ENERGY 9

Light and Nanotechnology, interaction of light and Nanotechnology, Nanoholes and photons, solar cells, optically useful Nanostructured polymers, photonic crystals.

UNIT V FUTURE APPLICATIONS 9

MEMS, Nanomachines, Nanodevices, Quantum Computers, Opto-electronic Devices, Quantum Electronic devices, environmental and biological applications.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: understand the bases for introduction to Nanotechnology

CO2: understand the synthesis of Nanomaterials and their application and the impact of Nanomaterials on environment

CO3: acquire knowledge about various kind of Nano materials

CO4: understand the Nanotechnology devices used and their structures

CO5: understand and improve the application of Nanotechnology

REFERENCES

1. Mick Wilson, Kamali Kannangra Geoff Smith, Michelle Simons and Burkhard Raguse,"Nanotechnology-Basic Science and Emerging Technologies", Overseas Press, 2002
2. Mark Ratner and Daniel Ratner, "Nanotechnology-a Gentle Introduction to The Next Big Idea",Prentice Hall,2003
3. Rebecca L Johnson,"Nanotechnology", Lerner Publications,2003

4. Charles P. Poole Jr., “Introduction to Nanotechnogy”,Chapman and Hall/CRS,2003

VL4007 EVOLVABLE HARDWARE L T P C
3 0 0 3

COURSE OBJECTIVES:

- To study about the evolvable systems algorithms, multi-objective utility functions
- Understand the concepts of reliability, design-in redundancy, fault tolerance and defect tolerance
- Design of evolvable systems using Programmable Logic Devices (like FPGAs) and modular subsystems with identical components and generalized controller algorithms

UNIT I INTRODUCTION 9

Traditional Hardware Systems and its Limitations, Evolvable Hardware, Characteristics of Evolvable Circuits and Systems, Technology-Extrinsic and Intrinsic Evolution offline and Online Evolution, Applications and Scope of EHW

UNIT II EVOLUTIONARY COMPUTATION 9

Fundamentals of evolutionary algorithms, components of EA, variants of EA, Genetic Algorithms, genetic programming, evolutionary strategies, evolutionary programming, implementations – evolutionary design and optimizations, EHW – current problems and potential solutions

UNIT III RECONFIGURABLE DIGITAL DEVICES 9

Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAS), using reconfigurable hardware – design phase, execution phase, evolution of digital circuits

UNIT IV RECONFIGURABLE ANALOG DEVICES 9

Basic architectures – Field Programmable Transistor Arrays (FPTAS), analog arrays, MWMS, using reconfigurable hardware – design phase, execution phase, evolution of analog circuits

UNIT V APPLICATIONS OF EHW 9

Synthesis vs. Adaptation, designing self-adaptive systems, fault-tolerant systems, real-time systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should will be able to:

CO1: understand the fundamentals of computational models and computers which have appeared at the intersection of hardware and artificial intelligence to solve hard computational problems.

CO2: understand the principles of bio-inspired and unconventional computational systems.

CO3: discuss about the reconfigurable digital architectures and its computational intelligence techniques.

CO4: discuss about the reconfigurable analog architectures and its computational intelligence techniques.

CO5: discuss about the typical applications of bio-inspired and other unconventional techniques in the phase of design, implementation and runtime of a computational device.

REFERENCES

1. Garrison W. Greenwood and Andrew M. Tyhrrell, “Introduction to Evolvable Hardware: a Practical Guide for Designing Self- Adaptive Systems”, Wiley-Ieee Press, 2006.

2. Tetsuya Higuchi, Xin Yao and Yong Liu, “Evolvable Hardware”, Springer-Verlag, 2004.
3. Lukas Sekanina, “Evolvable Components: From Theory to Hardware Implementations”, Springer, 2004

VL4092 SOFT COMPUTING AND OPTIMIZATION TECHNIQUES L T P C
3 0 0 3

COURSE OBJECTIVE:

- To classify various soft computing frame works.
- To be familiar with the design of neural networks, fuzzy logic, and fuzzy systems.
- To learn mathematical background for optimized genetic programming.
- Be exposed to neuro-fuzzy hybrid systems and its applications.
- To understand the various evolutionary optimization techniques.

UNIT I FUZZY LOGIC: 9

Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy sets- Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic.

UNIT II ARTIFICIAL NEURAL NETWORKS: 9

Supervised Learning: Introduction and how brain works, Neuron as a simple computing element, The perceptron, Backpropagation networks: architecture, multilayer perceptron, backpropagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network.

Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self- Organizing Computational Maps: Kohonen Network.

UNIT III GENETIC ALGORITHM: 9

Genetic algorithm- Introduction - biological background - traditional optimization and search techniques - Genetic basic concepts - operators – Encoding scheme – Fitness evaluation – crossover - mutation - Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

UNIT IV NEURO-FUZZY MODELING 9

Adaptive Neuro-Fuzzy Inference Systems (ANFIS) – architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – the inverted pendulum system.

UNIT V CONVENTIONAL OPTIMIZATION TECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton’s Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

TOTAL :45 PERIODS

COURSE OUTCOMES:

Upon Completion of the course, the students will be able to:

CO1: Develop application on different soft computing techniques like Fuzzy, GA and Neural network

CO2: Implement Neuro-Fuzzy and Neuro-Fuzz-GA expert system.
CO3: Implement machine learning through Neural networks.
CO4: Model Neuro Fuzzy system for clustering and classification.
CO5: Able to use the optimization techniques to solve the real world problems

REFERENCES:

1. J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI / Pearson Education 2004.
2. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
3. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 1995.
4. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2003.
5. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2003.
6. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.
7. Simon Haykins, Neural Networks: A Comprehensive Foundation, Prentice Hall International Inc, 1999.
8. Timothy J.Ross, Fuzzy Logic with Engineering Applications, McGraw-Hill, 1997.

VL4072 CAD FOR VLSI DESIGN L T P C
3 0 2 4

COURSE OBJECTIVES:

- to introduce the VLSI design methodologies and design methods.
- to introduce data structures and algorithms required for VLSI design.
- to study algorithms for partitioning and placement.
- to study algorithms for floor planning and routing.
- to study algorithms for modelling, simulation and synthesis.

UNIT I INTRODUCTION 9

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Review of VLSI Design Automation Tools

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS 9

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT 9

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

UNIT IV ALGORITHMS FOR FLOORPLANNING AND ROUTING 9

Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing – Global Routing – Detailed Routing.

UNIT V MODELLING, SIMULATION AND SYNTHESIS 9

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of this course, the students should be able to:

CO1: use various VLSI design methodologies

CO2: understand different data structures and algorithms required for VLSI design.

CO3: develop algorithms for partitioning and placement.

CO4: develop algorithms for floorplanning and routing.

CO5: design algorithms for modelling, simulation and synthesis.

REFERENCES

1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.
2. Naveed a. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Springer, 2017.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2.
4. N.a. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

VL4009 VLSI ARCHITECTURES FOR IMAGE PROCESSING L T P C

3 0 2 4

COURSE OBJECTIVES:

- The students will be able to acquire knowledge on image and video processing algorithms
- The students will be able to acquire knowledge on design of VLSI architectures.

UNIT I IMAGE PROCESSING ALGORITHMS AND ARCHITECTURES 9

Image Processing Tasks - Low Level Image Processing Operations - Intermediate Level Operations Image Processor Architecture: Requirements and Classification - Uni and Multi Processors - MIMD Systems - SIMD Systems - Pipelines - Design Aspects of Real Time Low Level Image Processors - Design Method for Special Architectures

UNIT II 3D IMAGE PROCESSING 9

Overview of 3D Image - Types and Characteristics of 3D Image Processing - Examples of 3D Image Processing, Continuous and Digitized Images, Models of Image Operations, Algorithm of Image Operations - Smoothing Filter - Difference Filter - Differential Features of a Curved Surface - Region Growing.

UNIT III 3D BINARY IMAGE PROCESSING 9

Introduction- Labeling of a Connected - Shrinking- Surface Thinning and Axis Thinning-Distance Transformation and Skeleton-Border Surface Following-Knot and Link .- Voronoi Division of a Digitized Image-Algorithms for Processing Connected Components with Gray Values

UNIT IV PIPELINED, 2D AND 3D IMAGE PROCESSING ARCHITECTURES 9

Architecture of a Cellular Logic Processing Element - Second Decomposition in Data Path and Control - Real Time Pipeline for Low Level Image Processing - Design Aspects of Image Processing Architectures - Implementation of Low Level 2D and 3D and Intermediate Level Algorithms

UNIT V VLSI SYSTEMS FOR IMAGE PROCESSING 9

Concurrent Systems for Image Analysis- VLSI Wavefront Arrays for Image Processing-Curve Detection in VLSI-Design of VLSI Based Multicomputer Architecture for Dynamic Scene Analysis-VLSI-Based Image Resampling for Electronic Publishing

TOTAL:45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Convert a 2D Image to 3D Image.
2. Perform Urinary, Binary Image Operations and Monotonic, Shift, Point, Shift-Invariant Operators for 2D Image.
3. Obtain a CT Scan Image , Perform The Following
   a. Smooth Filter
   b. Detection Filter
   c. Morphological Filter
   d. Region Growing
4. Perform Surface Thinning and Axis Thinning, Distance Transformation and Skeleton, Voronoi Division of a Digitized Image

TOTAL:30+45=75 PERIODS

COURSE OUTCOMES:

Upon Completion of The Course, Students Will Be Able to Demonstrate An Ability to

CO1: Analyze Various Architectures to Realize Image Processing Algorithms and Explain The 3D Image Processing Algorithms

CO2: Explore Various Processing Techniques of Image and Design Different Architectures for Image Processing.

CO3: Analyze various pipelined hardware architecture for 2D and 3D Image processing

CO4: Realize binary image processing algorithm in VLSI systems

CO5: Implement filter techniques in 2D and 3D image.

REFERENCES

1. Pieter Jonker, "Morphological Image Processing: Architecture and VLSI Design", Springer, First Edition, 1992.
2. Junichiro Toriwaki · Hiroyuki Yoshida, "Fundamentals of Three-Dimensional Digital Image Processing", Springer 2009.
3. King-Sun Fu, "VLSI for Pattern Recognition and Image Processing", Springer-Verlag, 1984.

VL4010 **SYSTEM VERILOG** **L T P C**
3 0 2 4

COURSE OBJECTIVES:

- Insight to Apply System Verilog Concepts to Do Synthesis, Analysis and Architecture Design.
- Understanding of System Verilog and SVA for Verification and Understand The Improvements in Verification Efficiency.
- Understand Advanced Verification Features, Such As The Practical Use of Classes, Randomization, Checking, and Coverage.
- Knowledge to Communicate The Purpose and Results of a Design Experiment in Written and Oral
- Understand The Purpose of Hardware-Software Verification

UNIT I VERIFICATION METHODOLOGY 9

Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench

UNIT II SYSTEM VERILOG BASICS AND CONCEPTS 9

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types With Typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions

UNIT III OOPS 9

Introduction-Where to Define a Class- OOPS Terminology -Creating New Objects -Object Deallocation- Using Objects -Static Variables Vs. Global Variables -Class Routines -Defining Routines Outside of The Class - Scoping Rules -Using One Class Inside Another - Understanding Dynamic Objects -Copying Objects -Public Vs. Private -Straying Off Course - Building a Testbench

UNIT IV THREADS AND INTER-PROCESS COMMUNICATION AND FUNCTIONAL COVERAGE 9

Working With Threads, Inter-Process Communication, Events, Semaphores, Mailboxes, Building a Testbench With Threads and IPC. Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analysing Coverage Data, Measuring Coverage Statistics

UNIT V COMPLETE DESIGN MODEL USING SYSTEM VERILOG- CASE STUDY 9

System Verilog ATM Example, Data Abstraction, Interface Encapsulation, Design Top Level Squat, Receivers and Transmitters, Test Bench for ATM.

TOTAL:45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Design a Testbench for 2x1 Mux Using Gates
2. Implementation of a Mailbox By Allocating Memory
3. Implementation and Testing of Semaphore for a Simple DUT
4. Implementation of Scoreboard for a Simple DUT

TOTAL:45+30=45 PERIODS

COURSE OUTCOMES:

Upon completion of this course, students should demonstrate the ability to

CO1: use system 52erilog to create correct, efficient, and re-usable models for digital designs

CO2: use system 52erilog to create testbenches for digital designs

CO3: understand and effectively exploit new constructs in System Verilog for verification

CO4: understand the communication between modules

CO5: designing a complete system model using Verilog

REFERENCES

1. System Verilog for Verification: a Guide to Learning The Testbench Language Features, Chris Spear,Springer 2006
2. Writing Testbenches: Functional Verification of HDL Models, Second Edition, Janick Bergeron, Kluwer Academic Publishers, 2003.
3. System Verilog for Design: a Guide to Using System Verilog for Hardware Design and Modeling, 2nd Edition, Stuart Sutherland, Simon Davidman and Peter Flake, Springer
4. Open Verification Methodology Cookbook, Mark Glasser, Springer, 2009
5. Assertion-Based Design, 2nd Edition, Harry D. Foster, Adam C. Krolnik, David J. Lacey, Kluwer Academic Publishers, 2004

VL4011 ADAPTIVE SIGNAL PROCESSING L T P C

3 0 2 4

COURSE OBJECTIVES:

- to understand the basic principles of discrete random signal processing
- to understand the principles of spectral estimation
- to learn about the weiner and adaptive filters
- to understand the different signal detection and estimation methods
- to acquire skills to design synchronization methods for proper functioning of the system

UNIT I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes, Random Variables, Parseval's Theorem, Wiener-Khintchine Relation, Power Spectral Density, Spectral Factorization, Filtering Random Processes, Special Types of Random Processes

UNIT II SPECTRAL ESTIMATION 9

Introduction, Nonparametric Methods – Periodogram, Modified Periodogram, Bartlett, Welch and Blackman-Tukey Methods, Parametric Methods – ARMA, AR and MA Model Based Spectral Estimation, Solution Using Levinson-Durbin Algorithm.

UNIT III WEINER AND ADAPTIVE FILTERS 9

Weiner Filter: FIR Wiener Filter, IIR Wiener Filter, Adaptive Filter: FIR Adaptive Filters – Steepest Descent Method- LMS Algorithm, RLS Adaptive Algorithm, Applications.

UNIT IV DETECTION AND ESTIMATION 9

Bayes Detection Techniques, Map, Ml,– Detection of M-Ary Signals, Neymanpearson, Minimax Decision Criteria. Kalman Filter- Discrete Kalman Filter, The Extended Kalman Filter, Application.

UNIT V SYNCHRONIZATION 9

Signal Parameter Estimation, Carrier Phase Estimation, Symbol Timing Estimator, Joint Estimation of Carrier Phase and Symbol Timing.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Design of Non- Parametric and Parametric for Spectral Estimation
2. Design of Linear Prediction Filter Using Matlab
3. Design of LMS Filter Using Matlab
4. Design of RLS Filter Using Matlab
5. Design of Extended Kalman Filter Using Matlab

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basic principles of discrete random signal processing

CO2:Analyze the principles of spectral estimation

CO3:Analyze the Weiner and Adaptive filters

CO4:Analyze the different signal detection and estimation methods

CO5:Design the synchronization methods for proper functioning of the system

REFERENCES

1. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons, Inc, Singapore, 2009.
2. John G. Proakis., “Digital Communication”, 4th Edition, McGraw Hill Publications, 2001.
3. Simon Haykin, “Adaptive Filter Theory”, Pearson Education, Fourth Edition, 2003
4. Bernard Sklar and Pabitra Kumar Roy, “Digital Communications: Fundamentals and Applications”, 2/E, Pearson Education India, 2009
5. Paulo S. R. Diniz, “Adaptive Filtering Algorithms and Practical Implementation”, Springer, 2011

CP4252 MACHINE LEARNING L T P C

3 0 2 4

COURSE OBJECTIVES:

- To understand the concepts and mathematical foundations of machine learning and types of problems tackled by machine learning
- To explore the different supervised learning techniques including ensemble methods
- To learn different aspects of unsupervised learning and reinforcement learning
- To learn the role of probabilistic methods for machine learning
- To understand the basic concepts of neural networks and deep learning

UNIT I INTRODUCTION AND MATHEMATICAL FOUNDATIONS 9

What is Machine Learning? Need –History – Definitions – Applications – Advantages, Disadvantages & Challenges –Types of Machine Learning Problems – Mathematical Foundations – Linear Algebra & Analytical Geometry –Probability and Statistics- Bayesian Conditional Probability -Vector Calculus & Optimization – Decision Theory – Information theory

UNIT II SUPERVISED LEARNING 9

Introduction-Discriminative and Generative Models –Linear Regression - Least Squares –Under-fitting

/ Overfitting –Cross-Validation – Lasso Regression- Classification - Logistic Regression- Gradient Linear Models –Support Vector Machines –Kernel Methods –Instance based Methods – K-Nearest Neighbours – Tree based Methods –Decision Trees –ID3 – CART – Ensemble Methods –Random Forest – Evaluation of Classification Algorithms

UNIT III UNSUPERVISED LEARNING AND REINFORCEMENT LEARNING 9

Introduction – Clustering Algorithms –K – Means – Hierarchical Clustering – Cluster Validity – Dimensionality Reduction –Principal Component Analysis – Recommendation Systems - EM algorithm. Reinforcement Learning – Elements –Model based Learning – Temporal Difference Learning

UNIT IV PROBABILISTIC METHODS FOR LEARNING- 9

Introduction –Naïve Bayes Algorithm –Maximum Likelihood –Maximum Apriori –Bayesian Belief Networks –Probabilistic Modelling of Problems –Inference in Bayesian Belief Networks – Probability Density Estimation – Sequence Models – Markov Models – Hidden Markov Models

UNIT V NEURAL NETWORKS AND DEEP LEARNING 9

Neural Networks – Biological Motivation- Perceptron – Multi-layer Perceptron – Feed Forward Network – Back Propagation-Activation and Loss Functions- Limitations of Machine Learning – Deep Learning– Convolution Neural Networks – Recurrent Neural Networks – Use cases

45 PERIODS

SUGGESTED ACTIVITIES:

1. Give an example from our daily life for each type of machine learning problem
2. Study at least 3 Tools available for Machine Learning and discuss pros & cons of each
3. Take an example of a classification problem. Draw different decision trees for the example and explain the pros and cons of each decision variable at each level of the tree
4. Outline 10 machine learning applications in healthcare
5. Give 5 examples where sequential models are suitable.
6. Give at least 5 recent applications of CNN

PRACTICAL EXERCISES: 30 PERIODS

1. Implement a Linear Regression with a Real Dataset (https://www.kaggle.com/harrywang/housing). Experiment with different features in building a model. Tune the model's hyperparameters.
2. Implement a binary classification model. That is, answers a binary question such as "Are houses in this neighborhood above a certain price?"(use data from exercise 1). Modify the classification threshold and determine how that modification influences the model. Experiment with different classification metrics to determine your model's effectiveness.
3. Classification with Nearest Neighbours. In this question, you will use the scikit-learn's KNN classifer to classify real vs. fake news headlines. The aim of this question is for you to read the scikit-learn API and get comfortable with training/validation splits. Use California Housing Dataset
4. In this exercise, you'll experiment with validation sets and test sets using the dataset. Split a training set into a smaller training set and a validation set. Analyze deltas between training set and validation set results. Test the trained model with a test set to determine whether your trained model is overfitting. Detect and fix a common training problem.
5. Implement the k-means algorithm using https://archive.ics.uci.edu/ml/datasets/Codon+usage dataset
6. Implement the Naïve Bayes Classifier using

https://archive.ics.uci.edu/ml/datasets/Gait+Classification dataset

7. Project - (in Pairs) Your project must implement one or more machine learning algorithms and apply them to some data.
    a. Your project may be a comparison of several existing algorithms, or it may propose a new algorithm in which case you still must compare it to at least one other approach.
    b. You can either pick a project of your own design, or you can choose from the set of pre-defined projects.
    c. You are free to use any third-party ideas or code that you wish as long as it is publicly available.
    d. You must properly provide references to any work that is not your own in the write-up.
    e. Project proposal You must turn in a brief project proposal. Your project proposal should describe the idea behind your project. You should also briefly describe software you will need to write, and papers (2-3) you plan to read.

List of Projects (datasets available)

1. Sentiment Analysis of Product Reviews
2. Stock Prediction
3. Sales Forecasting
4. Music Recommendation
5. Handwriting Digit Classification
6. Fake News Detection
7. Sports Prediction
8. Object Detection
9. Disease Prediction

COURSE OUTCOMES:

Upon the completion of course, students will be able to

CO1: Understand and outline problems for each type of machine learning

CO2: Design a Decision tree and Random forest for an application

CO3: Implement Probabilistic Discriminative and Generative algorithms for an application and analyze the results.

CO4: Use a tool to implement typical Clustering algorithms for different types of applications.

CO5: Design and implement an HMM for a Sequence Model type of application and identify applications suitable for different types of Machine Learning with suitable justification.

TOTAL:75 PERIODS

REFERENCES

1. Stephen Marsland, “Machine Learning: An Algorithmic Perspective”, Chapman & Hall/CRC, 2nd Edition, 2014.
2. Kevin Murphy, “Machine Learning: A Probabilistic Perspective”, MIT Press, 2012
3. Ethem Alpaydin, “Introduction to Machine Learning”, Third Edition, Adaptive Computation and Machine Learning Series, MIT Press, 2014
4. Tom M Mitchell, “Machine Learning”, McGraw Hill Education, 2013.
5. Peter Flach, “Machine Learning: The Art and Science of Algorithms that Make Sense of Data”, First Edition, Cambridge University Press, 2012.
6. Shai Shalev-Shwartz and Shai Ben-David, “Understanding Machine Learning: From Theory to Algorithms”, Cambridge University Press, 2015
7. Christopher Bishop, “Pattern Recognition and Machine Learning”, Springer, 2007.
8. Hal Daumé III, “A Course in Machine Learning”, 2017 (freely available online)
9. Trevor Hastie, Robert Tibshirani, Jerome Friedman, “The Elements of Statistical Learning”,

Springer, 2009 (freely available online)
10. Aurélien Géron , Hands-On Machine Learning with Scikit-Learn and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems 2nd Edition, o'reilly, (2017)

DS4151 DIGITAL IMAGE AND VIDEO PROCESSING L T P C
3 0 2 4

COURSE OBJECTIVES:

- To provide the student with basic understanding of image fundamentals and transforms
- To provide exposure to the students about image enhancement and restoration
- To impart a thorough understanding about segmentation and Recognition.
- To know the Video Processing and motion estimation
- Learning the concepts will enable students to design and develop an image processing application .

UNIT I FUNDAMENTALS OF IMAGE PROCESSING AND TRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform ,Walsh transform, Hadamard transform, Haar transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms. Digital Camera working principle.

UNIT II ENHANCEMENT AND RESTORATION 9

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters. Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Introduction to Image restoration, Image degradation, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution. Color image enhancement.

UNIT III SEGMENTATION AND RECOGNITION 9

Edge detection, Edge linking via Hough transform – Thresholding – Region based segmentation – Region growing – Region splitting and merging – Morphological processing- erosion and dilation, Boundary representation, Boundary description, Fourier Descriptor, Regional Descriptors – Topological feature, Texture – Patterns and Pattern classes – Recognition based on matching.

UNIT IV BASIC STEPS OF VIDEO PROCESSING 9

Analog Video, Digital Video. Time-Varying Image Formation models:Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation,Sampling of Videosignals, Filtering operations

UNIT V 2-D MOTION ESTIMATION 9

Optical flow, optical flow constraints, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based MotionEstimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding,Predictive coding, Application of motion estimation in Video coding.

45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

1. Histogram Equalization

2. Image Filtering (spatial-domain)
3. Image Filtering (frequency-domain)
4. Image Segmentation
5. Familiarization with Video Processing tools
6. Denoising video
7. Video resizing
8. Background subtraction
9. Interpolation methods for re-sampling
10. Adaptive unsharp masking based interpolation for video up-sampling
11. Gaussian mixture model (GMM) based background subtraction
12. Video encoding

COURSE OUTCOMES:

On the successful completion of the course, students will be able to

CO1: Analyze the digital image, representation of digital image and digital images in transform Domain.

CO2: Analyze the detection of point, line and edges in images and understand the redundancy in images, various image compression techniques.

CO3: Analyze the video technology from analog color TV systems to digital video systems, how video signal is sampled and filtering operations in video processing.

CO4: Obtain knowledge in general methodologies for 2D motion estimation, various coding used in video processing.

CO5: Design image and video processing systems.

TOTAL:75 PERIODS

REFERENCES:

1. Digital Image Processing – Gonzalez and Woods, 3rd Ed., Pearson, 2016
2. Handbook of Image and Video processing, Academic press, 2010
3. K.R.Castelman, Digital Image processing, Prentice Hall, 1996
4. Anil Kumar Jain, Fundamentals of Digital Image Processing, Prentice Hall of India.2nd edition, 2002
5. R C Gonzalez, R E Woods and S L Eddins, Digital Image Processing Using Matlab, Pearson Education , 2006

AUDIT COURSES

AX4091 ENGLISH FOR RESEARCH PAPER WRITING **L T P C**
2 0 0 0

COURSE OBJECTIVES:

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING **6**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS 6

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS 6

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS 6

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS 6

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES:

CO1 –Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

REFERENCES:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX4092 DISASTER MANAGEMENT L T P C

2 0 0 0

COURSE OBJECTIVES:

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

COURSE OUTCOMES:

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO5: Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX4093 **CONSTITUTION OF INDIA** **L T P C**
2 0 0 0

COURSE OBJECTIVES:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION

History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist

Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.

- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX4094 **நற்றமிழ் இலக்கியம்** **L T P C**
2 0 0 0

UNIT I **சங்க இலக்கியம்** **6**

1. தமிழின் துவக்க நூல் தொல்காப்பியம்
   – எழுத்து, சொல், பொருள்
2. அகநானூறு (82)
   - இயற்கை இன்னிசை அரங்கம்
3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி
4. புறநானூறு (95,195)
   - போரை நிறுத்திய ஔவையார்

UNIT II **அறநெறித் தமிழ்** **6**

1. அறநெறி வகுத்த திருவள்ளுவர்
   - அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புறவு அறிதல், ஈகை, புகழ்
2. பிற அறநூல்கள் - இலக்கிய மருந்து
   – ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

UNIT III **இரட்டைக் காப்பியங்கள்** **6**

1. கண்ணகியின் புரட்சி
   - சிலப்பதிகார வழக்குரை காதை
2. சமூகசேவை இலக்கியம் மணிமேகலை
   - சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

UNIT IV **அருள்நெறித் தமிழ்** **6**

1. சிறுபாணாற்றுப்படை
   - பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்
2. நற்றிணை
   - அன்னைக்குரிய புன்னை சிறப்பு

3. திருமந்திரம் (617, 618)
   - இயமம் நியமம் விதிகள்
4. தர்மச்சாலையை நிறுவிய வள்ளலார்
5. புறநானூறு
   - சிறுவனே வள்ளலானான்
6. அகநானூறு (4) - வண்டு
   நற்றிணை (11) - நண்டு
   கலித்தொகை (11) - யானை, புறா
   ஐந்திணை 50 (27) - மான்

ஆகியவை பற்றிய செய்திகள்

UNIT V **நவீன தமிழ் இலக்கியம்** **6**

1. உரைநடைத் தமிழ்,
   - தமிழின் முதல் புதினம்,
   - தமிழின் முதல் சிறுகதை,
   - கட்டுரை இலக்கியம்,
   - பயண இலக்கியம்,
   - நாடகம்,
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும்,
5. அறிவியல் தமிழ்,
6. இணையத்தில் தமிழ்,
7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

TOTAL: 30 PERIODS

<u>தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்</u>

1. தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)
   - www.tamilvu.org
2. தமிழ் விக்கிப்பீடியா (Tamil Wikipedia)
   -https://ta.wikipedia.org
3. தர்மபுர ஆ**தீ**ன வெளியீடு
4. வாழ்வியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்
5. தமிழ்கலைக் களஞ்சியம்
   - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6. அறிவியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்